Abstract of the Disclosure

Soft errors occur during normal use of a solid-state memory such as EEPROM or Flash EEPROM. A soft error results from the programmed threshold voltage of a memory cell being drifted from its originally intended level. The error is initially not readily detected during normal read until the cumulative drift becomes so severe that it develops into a hard error. Data could be lost if enough of these hard errors swamps available error correction codes in the memory. A memory device and techniques therefor are capable of detecting these drifts and substantially maintaining the threshold voltage of each memory cell to its intended level throughout the use of the memory device, thereby resisting the development of soft errors into hard errors.